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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/030,175	01/31/2002	Simon Deleonibus	218207US2PCT	6232

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EXAMINER
PERALTA, GINETTE

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 11/20/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/030,175	Applicant(s) DELEONIBUS, SIMON	
	Examiner Ginette Peralta	Art Unit 2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

1. Claims 1 and 9 are objected to because of the following informalities:

The term "so-called" should be deleted from the claims.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-3, and 5-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boyd et al. (U. S. Pat. 6,271,094 B1) in view of Deleonibus (FR 2750534 A1).

Regarding claim 1, Boyd et al. teaches in figs. 2A to 2F a method for fabricating an electronic component with self-aligned source, drain and gate, that comprises the steps of forming a dummy gate (52, 36) on a silicon substrate (10), the dummy gate defining a position for a channel (30) of the component, at least one implantation of doping impurities in the substrate, to form a source and a drain on either side of the channel, using the dummy gate as implanting mask (col. 7, ll. 12-15), superficial, self-aligned siliciding of the source and drain (col. 7, ll. 16-20), depositing at least one layer of insulating layer 60 and polishing the layer stopping at the dummy gate, replacing

the dummy gate by at least one final gate separated from the substrate by a gate insulating layer62, and electrically insulated from the source and drain.

Boyd et al. shows all the limitations in the claim with the exception of depositing at least one layer of contact metal having a total thickness greater than the height of the dummy gate.

Deleonibus teaches in Fig. 9 and 10 a method for fabricating an electronic component that includes the steps of depositing at least one layer of contact metal having a total thickness greater than the height of the gate, and polishing the contact metal stopping on the gate, wherein the contact metal layer is formed for the disclosed intended purpose of forming self-aligned contacts to the source and drain regions.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form a metal contact layer and polish the layer stopping on the gate for the disclosed intended purpose of Deleonibus of forming self-aligned contacts to the source and drain regions.

Regarding claim 2, Boyd et al, as modified by Deleonibus above teaches depositing a first metal layer 125, and above the first layer, a second metal layer 148 having greater mechanical resistance to polishing than the first layer, the thickness of the first metal layer 125 being less than the height of the dummy gate, but the total thickness of the first and second layers being greater than the height of the dummy gate.

Regarding claim 3, Boyd et al. teaches in col. 8, ll. 6-10, forming the side spacers 32 on the sides of the dummy gate before siliciding.

Regarding claim 5, Boyd as modified by Deleonibus above, teaches the first metal comprising titanium or tungsten, and the second metal comprising tungsten.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use any other refractory material like tantalum, titanium, or molybdenum, among others, and alloys thereof, as the use of this materials is well known in the art and since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416.

Regarding claim 6, Boyd et al. teaches after polishing, the deposition of a metal oxide layer (col. 6, ll. 22-35). It would have been within the scope of one of ordinary skill in the art at the time the invention was made that when the metal oxide layer is deposited, under the conditions used, any other present metals, like titanium, tungsten, tantalum, would also be superficially oxidized.

Regarding claim 7, Boyd et al. teaches the use of a solid substrate.

Regarding claim 8, Boyd et al. does not specify the substrate used. Deleonibus teaches the use of silicon on insulator substrate. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use any type of semiconductor substrate like SOI or silicon, among others, as the use of this substrates is well known in the art and since it has been held to be within the general skill of a

worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416.

Regarding claim 9, Boyd et al. teaches that the step of removal of the dummy gate includes formation of a gate insulation layer 62, depositing a metal layer 28 as the gate layer, having an overall thickness equal to or greater than the height of the removed dummy gate, and forming the metal layer.

4. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Boyd et al. in view of Deleonibus as applied to claims 1-3, 5-10 above, and further in view of Misra et al. (U. S. Pat. 5,960,270).

Boyd et al. as modified by Deleonibus above, teaches all the limitations in the claim with the exception of the spacers being dual layer spacers comprising silicon oxide in contact with the dummy gate and a superficial layer of silicon nitride.

Misra et al. teaches a method of manufacturing a MOSFET utilizing a dummy gate, that discloses in fig. 12 dual-layer spacers that are formed comprising an attachment layer 112 of silicon oxide in contact with the dummy gate, and a superficial layer 114 comprising silicon nitride, wherein a dual layer is used as the spacers for the purpose of protecting the gate structure in further process steps.

Thus, it would have been within the scope of one of ordinary skill in the art at the time the invention was made to use a dual-layer as the one taught by Misra et al. for its intended purpose of protecting the gate electrode structure. Furthermore, it would have been obvious to one of ordinary skill in the art at the time the invention was made

to form a single or dual-layer spacers, since it has been held that omission of an element and its function in a combination where the remaining elements perform the same functions as before involves only routine skill in the art. *In re Karlson,* 136 USPQ 184.

5. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Boyd et al. in view of Deleonibus as applied to claims 1-3, 5-9 above, and further in view of Gardner et al. (U. S. Pat. 6,200,865 B1).

Boyd et al. as modified by Deleonibus above teaches all the limitations in the claim with the exception of depositing an inter-gate dielectric layer and a second gate metal layer.

Gardner et al. teaches a method of manufacturing a semiconductor device that includes the formation of a gate insulating layer 36, the deposition of a first gate metal layer 46, the deposition of one inter-gate dielectric layer 50, and the deposition of a second gate metal layer 56, wherein the structure is formed in this manner for the disclosed intended purpose of forming a dual gate structure that is useful in memory cells by decreasing the area of the device.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form a dual gate comprising a first and second metal layers, and an inter-gate dielectric in the invention of Boyd et al. for the disclosed intended purpose of Gardner et al. of forming a structure that decreases the size of the device by providing a dual gate that can be useful in memory devices.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ginette Peralta whose telephone number is (703)305-7722. The examiner can normally be reached on Monday to Friday 8:00 AM- 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (703)308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7722 for regular communications and (703)308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

GP
November 15, 2002

Wael Fahmy

SUPERVISORY PRIMARY EXAMINER
TECHNOLOGY CENTER 2800